What is claimed is:

1. A system for simulating a lithographic design comprised of a plurality of polygons arranged in a predetermined configuration, the system comprising:

a microprocessor subsystem to convert the plurality of polygons to a pixel-based bitmap representation thereof, wherein the pixel-based bitmap includes pixel data, and wherein each pixel datum represents a pixel having a predetermined pixel size; and

an accelerator subsystem, coupled to the microprocessor subsystem, to calculate at least a portion of an aerial image of the lithographic design using the pixel-based bitmap representation of the lithographic design, wherein the hardware accelerator subsystem includes a plurality of programmable gate arrays configured to process the pixel data in parallel.

2. The system of claim 1 wherein the pixel-based bitmap is a gray-level image which is representative of the plurality of polygons.

3. The system of claim 1 wherein the predetermined pixel size is greater than the Nyquist frequency in the aerial image of the lithographic design.

4. The system of claim 1 wherein the predetermined pixel size is determined using the numerical aperture and wavelength of a projection optics of a lithographic tool.

5. The system of claim 1 wherein the lithographic design includes resolution enhancement technology and wherein the microprocessor subsystem converts the plurality of polygons, including resolution enhancement technology, to a pixel-based bitmap representation thereof.

6. The system of claim 1 further including a plurality of accelerator subsystems, each accelerator subsystem being coupled to the microprocessor subsystem and provided a portion of the pixel-based bitmap to calculate an aerial image of the lithographic design corresponding to the portion of the pixel-based bitmap using the pixel data associated therewith.

7. The system of claim 6 wherein the microprocessor subsystem includes a plurality of microprocessors and wherein each microprocessor is coupled to at least one associated accelerator subsystem.

8. The system of claim 7 wherein the plurality of accelerator subsystems each performs Fast Fourier Transforms, using pixel data, to generate the corresponding portion of the aerial image.

9. The system of claim 1 wherein the accelerator subsystem calculates an aerial image in resist formed on a wafer by the lithographic design wherein the accelerator subsystem calculates the aerial image in resist using the pixel-based bitmap representation

of the lithographic design and a coefficient matrix representing projection and illumination optics of a lithographic tool.

10. The system of claim 9 wherein the accelerator subsystem calculates a pattern formed on the wafer by the lithographic design wherein the accelerator subsystem calculates the pattern on the wafer using the pixel-based bitmap representation of the lithographic design and the coefficient matrix representing projection and illumination optics of a lithographic tool.

11. The system of claim 10 further including a processing system, coupled to the microprocessor subsystem and the accelerator subsystem, to compare the calculated pattern on the wafer to a desired, predetermined pattern.

12. The system of claim 10 further including a processing system, coupled to the microprocessor subsystem and the accelerator subsystem, to determine a CD of the lithographic design using the calculated pattern on the wafer.

13. The system of claim 10 further including a processing system, coupled to the microprocessor subsystem and the accelerator subsystem, to determine an edge placement of the lithographic design using the calculated pattern on the wafer.

14. The system of claim 10 further including a processing system, coupled to the microprocessor subsystem and the accelerator subsystem, to determine a printing

sensitivity using patterns on the wafer calculated in response to varying the coefficients of the matrix representing projection and illumination optics of a lithographic tool.

15. The system of claim 14 wherein the coefficients of the matrix representing projection and illumination optics of a lithographic tool are representative of one or more of a focus, dose, numerical aperture, illumination aperture, and aberration.

16. The system of claim 15 wherein the processing system determines a set of parameters of the projection and illumination optics of the lithographic tool using the printing sensitivity.

17. The system of claim 10 further including a processing system, coupled to the microprocessor subsystem and the accelerator subsystem, to detect an error in the lithographic design in response to a comparison between the calculated pattern on the wafer and a desired, predetermined pattern.

18. The system of claim 17 wherein, in response to detecting the error, the processing system determines a modification to the lithographic design to correct the error in the lithographic design.

19. A system for simulating a lithographic design, the system comprising:

a microprocessor subsystem, including a plurality of microprocessors, to convert the lithographic design to a pixel-based bitmap representation thereof,

wherein the pixel-based bitmap includes pixel data, and wherein each pixel datum represents a pixel having a predetermined pixel size; and

a plurality of accelerator subsystems, each accelerator subsystem includes a plurality of programmable integrated circuits configured to process the pixel data in parallel and each accelerator subsystem is connected to an associated microprocessor to calculate a portion of an aerial image of the lithographic design using the corresponding portion of the pixel-based bitmap representation of the lithographic design.

20. The system of claim 19 wherein the lithographic design is comprised of a plurality of polygons arranged in a predetermined configuration.

21. The system of claim 20 wherein the pixel-based bitmap is a gray-level image which is representative of the plurality of polygons.

22. The system of claim 19 wherein the predetermined pixel size is greater than the Nyquist frequency in the aerial image of the lithographic design.

23. The system of claim 19 wherein the predetermined pixel size is determined using the numerical aperture and wavelength of a projection optics of a lithographic tool.

24. The system of claim 19 wherein the lithographic design includes resolution enhancement technology and wherein the microprocessor subsystem converts the plurality

of polygons, including resolution enhancement technology, to a pixel-based bitmap representation thereof.

25. The system of claim 19 wherein the plurality of accelerator subsystems each performs Fast Fourier Transforms, using pixel data, to generate the corresponding portion of the aerial image.

26. The system of claim 19 wherein the plurality of accelerator subsystems calculate an aerial image in resist formed on a wafer by the lithographic design, wherein the accelerator subsystems calculate the aerial image in resist using the pixel-based bitmap representation of the lithographic design and a coefficient matrix representing projection and illumination optics of a lithographic tool.

27. The system of claim 26 wherein the accelerator subsystems calculate a pattern formed on the wafer by the lithographic design wherein the accelerator subsystems calculate the pattern on the wafer using the pixel-based bitmap representation of the lithographic design and the coefficient matrix representing projection and illumination optics of a lithographic tool.

28. The system of claim 27 further including a processing system, coupled to the microprocessor subsystems and the accelerator subsystems, to compare the calculated pattern on the wafer to a desired, predetermined pattern.

29. The system of claim 27 further including a processing system, coupled to the microprocessor subsystems and the accelerator subsystems, to determine a CD of the lithographic design using the calculated pattern on the wafer.

30. The system of claim 27 further including a processing system, coupled to the microprocessor subsystems and the accelerator subsystems, to determine an edge placement of the lithographic design using the calculated pattern on the wafer.

31. The system of claim 27 further including a processing system, coupled to the microprocessor subsystems and the accelerator subsystems, to determine a printing sensitivity using patterns on the wafer calculated in response to varying the coefficients of the matrix representing projection and illumination optics of a lithographic tool.

32. The system of claim 31 wherein the coefficients of the matrix representing projection and illumination optics of a lithographic tool are representative of one or more of a focus, dose, numerical aperture, illumination aperture, and aberration.

33. The system of claim 32 wherein the processing system determines a set of parameters of the projection and illumination optics of the lithographic tool using the printing sensitivity.

34. The system of claim 27 further including a processing system, coupled to the microprocessor subsystems and the accelerator subsystems, to detect an error in the

lithographic design in response to a comparison between the calculated pattern on the wafer and a desired, predetermined pattern.

35. The system of claim 34 wherein, in response to detecting the error, the processing system determines a modification to the lithographic design to correct the error in the lithographic design.